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On theFPGA Implementation of Binary Phase-ShiftKeying baseband Modem

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Abstract : In this paper, we implement a binary phase-shift keying (BPSK) modulation baseband communication MODEM using FPGA.We analyze and compare the theoretical bit error rate (BER), the computer simulated BER, and the BER obtained through the modem hardware implemented by FPGA in AWGN channel environments. A floating-point BER performance is determined using a MATLAB simulation. In order to obtain the performance of the MODEMhardware based on the fixed-point operation, we first predict the MODEMhardware output using a software package 'Modelsim' and then measure the actual bit error at the output of the FPGA hardware.Our experimental results show that the theoretical floating-point BERis 0.5dBsuperior to the measured fixed-point BER of MODEM hardware when the internal register of the FPGA is restrictedto 10 bits. It is also observed that the performance difference is reduced as the number of bits of the FPGA internal registers increases.

Keywords: binary phase-shift keying, MODEM, FPGA, internal register, bit error rate

I. INTRODUCTION

As we enter the 21st IT century, whenever and whereverpeople wantto get fast and reliable communication speeds and ubiquitous environment to send and receive data with the other party. For this purpose, sending and receiving data through a wireless and a reliablemodulator/demodulator (MODEM) technology is an essential element indispensable for such a ubiquitous network configurations. In addition to other transmission devices and stable performance of the modem, it has become a very important technical element forsuccessful ubiquitous environments.

Wired and wireless internet as well as throughout the digital communication research to improve the performance of the MODEM is a technical process which must be performed. At this time, application specific integrated circuit (ASIC) chip of the design process is that the middle field programmable gate array (FPGA) is a programmable semiconductor device as an AND Gate, OR gate Logic Gate, and so a number of programming a universal connection to a semiconductor. When using such a FPGA, as well as to easily design the semiconductor chip, unlike the general ASIC chip, so line editing is possible to try using when designing, implementing a real baseband modem immediately experiment, verified the theoretical results of these FPGA there are number of advantages.

The binary phase-shift keying (BPSK) modulation used by the MODEM implementation scheme is the most basic way of the communication modulation. In this paper, such a binary phase modulation method of the determined bit through simulation and theoretical bit error rate (BER) and another comparison in additive white addition Gaussian (AWGN) channel environment the bit error rate obtained from the baseband MODEM hardware implemented in the actual FPGA, analyzed, FPGA whether improvements were implemented during the study.

II. FPGA IMPLEMENTATION OF BPSK COMMUNICATION SYSTEMS

In this paper we construct a base module, as shown in Fig. 1 in order to implement the baseband modem using binary phase modulation communication system in FPGA. It was converted to the data - 1 first information 0 to obtain a random data was used as the PN generator, the bit information of 0 and + 1, through the line coding. The converted data is modulated in a binary phase modulation method passes through the root raised cosine (RRC) filter. RRC filter was used to reduce the distortion of the signal caused by passing through the modulated signal is bandwidth limited channel.

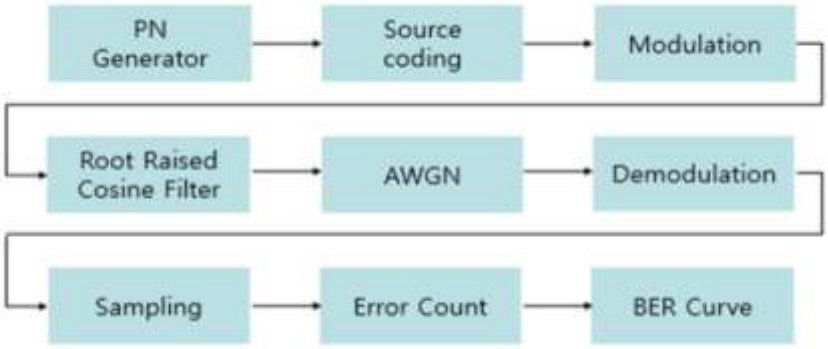

Fig. 1 Block diagram of each communication module for implementing FPGA

That is, the signal transmission at high data rates there is distortion in causing inter-symbol interference (ISI) between adjacent symbols, thereby the transmission signal transmitted through the pulse-like (pulse shaping) filter to eliminate the effect of this ISI. The purpose of this study was to remove the ISI between the signals affected by implementing the RRC filter. Adding white Gaussian transmission signal passing through the channel is demodulated using the correlation receiver at the receiving end. Correlation receiver is a method because it reduces the complexity of implementation, while the same operation as that of a matched filter that is worn by the actual hardware design.

III. BIT ERROR RATE SIMULATION OF BPSK SIGNAL

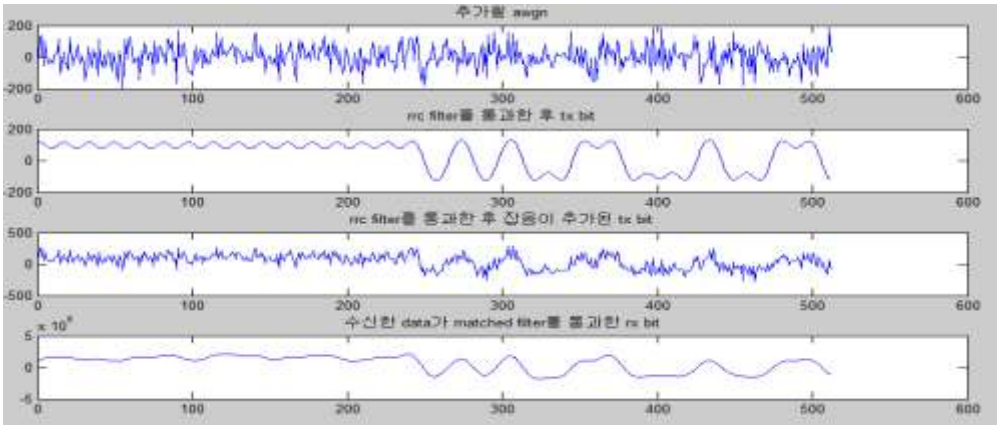

Fig. 2 Output signal of each module in the Matlab simulation process

In this study, we first carried out in MATLAB and '*Modelsim*' simulation for confirmation of the theoretical value required in the process using the FPGA to implement the modem and the actual behavior. The overall FPGA design method done the same to help configure each module as described in the preceding Fig. 1, it will be described in the simulation and implementation process based on MATLAB simulation, the most basic being the first in this section. First, the value of a variable associated declared in the first FPGA implementation, a PN generator is employed to generate random bit information. After this time the size is made of the arrangement 16 in each element were performed Exclusive OR operation, then if the if the value of the generated signal to the+ 1 after a process of converting a baseband binary phase-modulated by -1 the value of the modulated signal passed through the RRC filter. This process was taking the convolution operation to the modulated signal and the impulse response of the RRC filter in order to, by adding the noise signal generated by the output value of the RRC filter in AWGN module was generated input signal of the receiver end.

In the receiving end will go through the module to the demodulator demodulates the received signal, the demodulator was implemented as a correlation receiver as mentioned earlier form. Finally the bit error rate was measured by comparing the first information bit and the generated demodulated signal to confirm that was done correctly, the communication between the transmitted and received through it. Also we confirmed by a graphical representation of each parent output to verify that each module is operating properly.

We also consider a sync-related problem additionally while performing the simulation. Result subjected to convolution operation in the MATLAB implementation process is causing a slight operation delay within the FPGA. Therefore, the result values directly compared with the initial value of the information bit and reminds a lot of errors becomes excessive bit error rate increases accordingly. To solve this problem and to

better synchronize clock synchronization of the calculator the convolution results and the initial value of PN generator. This simulation process proceeds in the same manner as hardware verification using 'Modelsim', if only difference is Verilog attention to this when programming functions are not specified separately.

IV. SIMULATION RESULTS AND DISCUSSIONS

In this paper, using the MATLAB the blocks constituting the baseband modem performs a fixed-pointbased simulation, using the 'ModelSim' Simulator and its functions were designed to VerilogHDL Simulation Software. Simulation functions after using Altera's Quartus II were Synthesis with Altera Cyclone IV FPGA (EP4CE22F17C6N) chip. Reception of signal detection, timing synchronization is well done and the home was designed and transmit data is 16 bit Pseudorandom number generator to generate the 16 clock every one bit was sent to.

Source Coding was used for NRZ-L method, RRC filter is designed as Role-of-factor = 1, Symbol = 96. After performing convolution operation was input to the FPGA by AWGN noise is generated when the value of the MATLAB E_b / N_0 = 4~6 [dB]. Then samples the received data every 16 clocks found the error bit after the comparison of the transmitted data. FPAG board was used Terasic's DE0-Nano, it determines the number of bit errors by using the LED on the board. In experiments using a modem with a limited number of registers of the board to send and receive only 256 information bits were calculated bit error rate. Fig. 3 illustrates the process of determining an error by comparing the received data transmission.

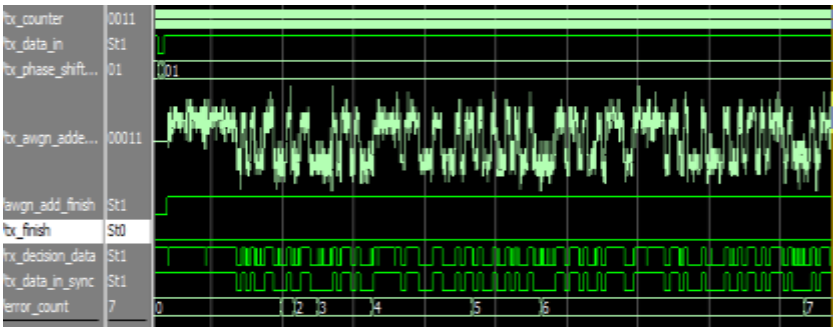

Fig. 3 Error simulation results

Fig. 4 compare the bit error rate, bit error rate measurement results by the simulation value and the actual modem implemented in FPGA based on floating-point operations. In FPGA there is the number of bits in the internal register limited shown a bit error rate performance based on fixed point operations, if the actual performance of the modem is limited to 8 bits can be seen to show a difference of about 0.3 dB compared to the theoretical value. The cause of this performance difference can be determined that the performance degradation due to analog-to-digital converter (ADC) fixed-point operation caused due to the restriction of the output bits that operates from an input end of the receiving end.

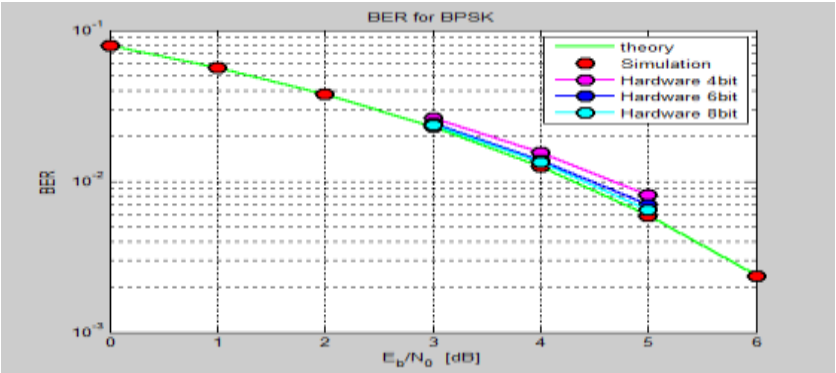

Fig. 4 Comparisonof BER performance

V. CONCLUSION

In this paper, we implement a BPSK baseband communication MODEM using FPGA and compared with the theoretical values by measuring BER. Experimental results of the BER performance of the hardware MODEM when limiting the internal registers are 8 bits was found that the difference between the theoretical value and remain approximately 0.3 dB or so. Future research will have a synchronization feature of the receiver, RF module, and so on.

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